A New Asymmetric Multilevel Inverter with Reduced Number of Components

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***Abstract*— This paper presents a new asymmetric voltage-source multilevel inverter with a reduced number of components. It is composed of several basic units, where each one can be designed to generate multilevel voltage with positive, zero, and negative levels. The basic units are connected in a cascaded fashion to provide the advantages of higher output voltage quality. To specify the amplitude of DC voltage source of the proposed inverter two methods are presented. Optimal topologies of the proposed inverter based on different criterions are also presented, which are important in the design process. The superiority of the proposed inverter is verified by comparison with some recent multilevel inverters in terms of IGBTs number, number of driver circuits, the total standing voltage on switches, and the number of output voltage levels. Losses analysis is also presented to study the effect of the modulation index and output power factor on the inverter efficiency. The ability of the proposed inverter to generate high-quality multilevel output voltage is verified through simulations and experimental results.**

***Index Terms*— Multilevel inverter, asymmetric topology, reduced components, cascaded connection.**

I. Introduction

Multilevel converters have received a great deal of attention from both industry and academic communities. Multilevel techniques not only improve the output power quality of the converter, but also have made it possible to achieve higher levels of voltage and power for the power electronic converters [1]. Higher power levels can be obtained using low-medium voltage semiconductor switches available in the market. To build a high power converter using traditional two-level converters, a serial connection of switches is mandatory. Advantages of multilevel converters open up a wide range of applications, such as UPS systems [2], hybrid PV-UPS system [3], traction [4], ship [5], renewable systems [6]-[7], drive [8]-[9], and power quality [10]-[11]. Despite unique features of multilevel converters, they usually use many switches, have more losses and cost, and complex modulation and control. Overcoming these issues is the subject of many research projects.

Multilevel converters can be classified into four groups in terms of number and voltage of DC voltage source(s), as the symmetrical, asymmetrical, hybrid, and single DC source multilevel converters [12]. Between these groups, some of multilevel symmetric and single DC source converters like cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) converters are known as traditional multilevel converters. Newer presented multilevel converters in the literature usually are derivation or combination of these classic converters. These converters consist of basic units, as the building block; by a series connection of the basic units, the output voltage levels of the converter will be increased.

In [13], a module consisting of the same DC voltage sources and bidirectional switches is introduced to create a stepped voltage with non-negative levels. It is shown that a higher number of voltage levels can be obtained by a series connection of these modules with different voltages. However, an H-bridge converter is necessary to generate negative voltage levels at the output for inverter applications. This topology has a lower number of gate driver circuits in comparison to cascaded H-bridge (CHB) inverter. In [14], a module named envelope type (E-Type) is presented as a building block and a multilevel inverter is proposed by the cascade connection of these E-Type modules. As this module generates positive, negative, and zero voltage levels, there is no need to use H-bridge converter at the output of the inverter. So, voltage stress on switches of the inverter can be reduced. As the amplitudes of DC voltage sources of the E-Type module are not equal, the presented inverter can be classified into asymmetrical multilevel converters group. A symmetric multilevel inverter consists of identical DC voltage sources is presented in [15], which offers lower power losses and fewer number of the DC voltage sources, on-state switches on the current path, as well as gate driver circuits. In [16], a multilevel inverter based on the series/parallel connection of identical DC voltage sources is presented that has a lower number of switches in comparison to the CHB multilevel inverter. This inverter uses a separated H-bridge converter with half voltage of the DC sources, so it is classified into hybrid multilevel converters. Using this inverter as a building block and by a series connection of them, another multilevel inverter can be obtained [17]. Due to the elimination of separated H-bridge and using modules with different DC voltage sources, this inverter is classified into asymmetrical multilevel converters. Also, it has a higher number of output voltage levels in comparison to the inverter presented in [16].

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In this paper, an asymmetrical multilevel inverter is proposed to improve the inverter presented in [17]. The proposed inverter enables the possibility of using DC voltage sources with different voltage amplitudes in each basic unit. Two analytic methods are developed to specify the amplitude of DC voltage sources. As a result, the proposed inverter provides a much higher number of output voltage levels and lower switch count.

II. Proposed Basic Unit

The proposed multilevel inverter consists of multipart that have similar functionalities with some different specifications. Fig. 1(a) shows proposed basic cell including two DC voltage sources (V_1 and V_2), two switches with unipolar voltage handling capability (S_m and S_l) and one switch with bipolar voltage handling capability (S_u). In this cell, V_2 is chosen to be greater than V_1 to create a building block for proposed asymmetric multilevel inverter. When S_l is in the on-state, to avoid short circuit fault on DC voltage sources, S_u has to be a bidirectional switch. The proposed basic cell can generate three voltage levels of V_1, V_2, and V_1+V_2. Combination of several basic cells, as shown in Fig.1 (b), can be used to generate a multilevel voltage. However, this voltage does not have any negative and zero levels. So, a Full-Bridge inverter (consists of $S_{1,1}$-$S_{1,4}$) has to be added to create a voltage waveform with all positive, zero, and negative levels. The basic unit of the proposed inverter is shown in Fig. 1 (b). In this paper, to determine voltage of the DC voltage sources in the proposed basic unit two methods are developed. In the first method to determine DC voltage sources amplitude for the basic unit, amplitudes of the DC voltage sources can be chosen as (1).

$$V_{1,j} = jV \quad , \quad j = 1,2,\dots,n_1, \tag{1}$$

where V and n_1 are the lowest value and number of DC voltage sources, respectively. The maximum number of output voltage levels (N_{step}) of the proposed basic unit can be achieved as,

$$N_{step} = n_1^2 + n_1 + 1. \tag{2}$$

The relation between the number of switches (N_{switch}) and DC voltage sources is as follows,

$$N_{switch} = 3n_1 + 1. \tag{3}$$

The standing voltage of each switch can be calculated as,

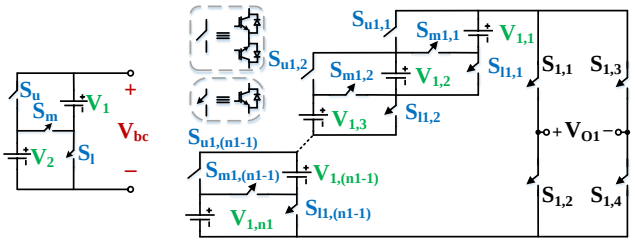
$$V_{S_{1,1}-S_{1,4}} = \sum_{i=1}^{n_1} V_{1,i}\,, \begin{cases} V_{S_{l1,i}} = V_{1,(i+1)} \\ V_{S_{m1,i}} = V_{1,(i+1)}, \\ V_{S_{u1,i}} = V_{1,i} \end{cases} i = 1,2,\dots,n_1 - 1. \tag{4}$$

Total standing voltage (TSV) of the proposed basic unit can be obtained by summation of standing voltage of each switch using (4). Therefore, one can write,

$$TSV = \left(\frac{7n_1^2 + 5n_1 - 4}{2}\right)V. \tag{5}$$

Maximum output voltage amplitude is as follows,

$$V_{O1,max} = \sum_{i=1}^{n_1} V_{1,i} = \frac{n_1(n_1+1)}{2}V. \tag{6}$$



(a) (b)

Fig. 1. Proposed inverter. (a) Basic cell, and (b) basic unit.

A switching table corresponding to the first method for the proposed basic unit is shown in Table I. The switches $S_{1,2}$/$S_{1,4}$ are compliments of $S_{1,1}$/$S_{1,3}$ that are not mentioned in this table.

In the second method to determine DC voltage sources amplitude for the basic unit, the amplitude of DC voltage sources of the proposed basic unit is calculated as,

$$V_{1,j} = \left(2^{j-1}\right)V\,, \quad j = 1,2,\dots,n_1. \tag{7}$$

In this method, the redundancy states are omitted and the maximum number of voltage levels can be achieved. Maximum number of voltage levels according to the second method is as follows,

$$N_{step} = 2^{n_1+1} - 1. \tag{8}$$

The standing voltage of each switch is the same as (4). The TSV of the basic unit is,

$$TSV = (13 \times 2^{n_1-1} - 9)V. \tag{9}$$

Maximum output voltage amplitude can be written as,

$$V_{O1,max} = \sum_{i=1}^{n_1} V_{1,i} = (2^{n_1} - 1)V. \tag{10}$$

By comparing (2) with (8), it can be concluded that the second method provides a higher number of levels than the first method. A switching table corresponding to the second method for the proposed basic unit can be obtained similar to Table I.

III. Proposed Multilevel Inverters

In this section, two inverters based on the cascade connection

TABLE I
SWITCHING TABLE OF THE BASIC UNIT FOR THE FIRST METHOD OF DETERMINING THE DC VOLTAGE SOURCE AMPLITUDES

Level or State	0	1	-1	2	3	.	$\frac{n_1(n_1+1)}{2}$	$-\frac{n_1(n_1+1)}{2}$
V_{O1}	0	V	$-V$	$2V$	$3V$	.	$\frac{n_1(n_1+1)}{2}V$	$-\frac{n_1(n_1+1)}{2}V$
$S_{1,1}$	1	1	0	1	1		1	0
$S_{1,3}$	1	0	1	0	0		0	1
$S_{u1,1}$	0	0	0	1	1		0	0
$S_{u1,2}$	0	0	0	0	1		0	0
⋮	0	0	0	0	0		0	0
$S_{u1,(n1-1)}$	0	0	0	0	0		0	0
$S_{m1,1}$	0	0	0	0	0		1	1
$S_{m1,2}$	0	0	0	0	0	.	1	1
⋮	0	0	0	0	0		1	1
$S_{m1,(n1-1)}$	0	0	0	0	0		1	1
$S_{l1,1}$	0	1	1	0	0		0	0
$S_{l1,2}$	0	1	1	1	0		0	0
⋮	0	1	1	1	1		0	0
$S_{l1,(n1-1)}$	0	1	1	1	1		0	0

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of the proposed basic units are presented, which are named as first and second proposed multilevel inverters. The basic structure of them is similar as shown in Fig. 2. The output voltage of these inverters is the sum of output voltages of all cascade connected basic units, as formulated in (11).

$$V_O(t) = \sum_{i=1}^{k} V_{O,i}(t). \tag{11}$$

Based on the two methods of determining DC voltage sources amplitudes of the basic unit, discussed in the previous section, two multilevel inverters are presented in the subsequent subsections.

A. First Proposed Multilevel Inverter

Amplitudes of the DC voltage sources in the first basic unit using the first method are as follows,

$$V_{1,1} = 1 \times V, \dots, V_{1,n_1} = n_1 \times V. \tag{12}$$

For the second basic unit we have,

$$\begin{aligned} V_{2,1} &= 2 \times \left(\sum_{i=1}^{n_1} V_{1,i} \right) + V = [n_1(n_1+1)+1] \times V, \\ &\vdots \\ V_{2,n_2} &= n_2 \times [n_1(n_1+1)+1] \times V. \end{aligned} \tag{13}$$

The general form for the j^{th} basic unit is as follows,

$$\begin{aligned} V_{j,1} &= 2 \times \left(\sum_{j=1}^{j-1} \sum_{i=1}^{n_j} V_{j,i} \right) + V = V \times \prod_{i=1}^{j-1} [n_i(n_i+1)+1], \\ &\vdots \\ V_{j,n_j} &= n_j \times V \times \prod_{i=1}^{j-1} [n_i(n_i+1)+1], \end{aligned} \tag{14}$$

where, $j = 2, \dots, k$. The maximum output voltage is

$$V_{o,max} = \frac{1}{2} \sum_{j=1}^{k} \left\{ n_j(n_j+1) \prod_{i=1}^{j-1} [n_i(n_i+1)+1] \right\} \times V. \tag{15}$$

The maximum number of output voltage levels now can be calculated as,

$$N_{step} = \prod_{i=1}^{k} [n_i(n_i+1)+1]. \tag{16}$$

B. Second Proposed Multilevel Inverter

To have optimal usage of switches, the amplitude of DC voltage sources is selected to generate output voltage levels without any redundancy. In this method, the amplitude of the DC voltage sources is calculated using geometrical progression with the ratio of two. For the first basic unit, one can write,

$$V_{1,1} = V, \dots, V_{1,n_1} = 2^{n_1-1} \times V. \tag{17}$$

For the second one, we have,

$$\begin{aligned} V_{2,1} &= 2 \times \left(\sum_{i=1}^{n_1} V_{1,i} \right) + V = (2^{n_1+1}-1) \times V, \\ &\vdots \\ V_{2,n_2} &= 2^{n_2-1} \times V_{2,1}. \end{aligned} \tag{18}$$

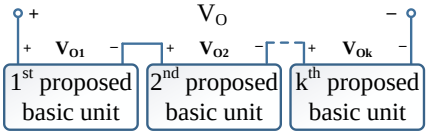

Fig. 2. Proposed multilevel structure.

In general, for the j^{th} basic unit we have,

$$V_{j,1} = V \times \prod_{i=1}^{j-1} [2^{n_i+1}-1], \dots, V_{j,n_j} = 2^{n_j-1} \times V_{j,1}, \tag{19}$$

where, $j = 2, \dots, k$. The maximum output voltage of the proposed multilevel inverter is as follows,

$$V_{o,max} = \sum_{j=1}^{k} \left[(2^{n_j}-1) \prod_{i=1}^{j-1} (2^{n_i+1}-1) \right] \times V. \tag{20}$$

Finally, the maximum number of output voltage levels can be calculated as,

$$N_{step} = \prod_{i=1}^{k} [2^{n_i+1}-1]. \tag{21}$$

C. Modulation Scheme

In order to have a desire voltage at the output of the proposed multilevel inverter, gate signals have to be generated according to a proper modulation scheme. To reduce the switching frequency, a modulation scheme based on the nearest level control (NLC) is presented here. In this scheme, the closest voltage level to the desired output voltage of the inverter is applied [18]. This modulation scheme is shown in Fig. 3. The normalized desired output voltage first scaled to the maximum number of output voltage levels in a half-cycle period, then the round function is applied to generate a staircase signal (u). An overall look-up table (LUT) that consider all possible switching states of the inverter is needed to specify what switches should be on/off in each instant according to u. The overall LUT is a combination of the basic units' switching states. As an example, for an inverter composed of two basic units with two DC voltage sources in each one (their amplitudes can be obtained from (14) and (19)), the overall LUT in the positive half-cycle of the output voltage is shown in Table II. The switching states of each basic unit are obtained from Table I. Switching states for the negative half-cycle can be produced using negative switching states of the second basic unit in the overall LUT. Finally, N_{IGBT} signals deliver to the gate driver circuits to modulate the switches of inverter. It is worth mentioning that the Sinusoidal-PWM scheme can also be used in the proposed inverter. However, this scheme leads to high switching losses in comparison with the nearest level control method.

IV. Optimal Structures For Proposed Multilevel Inverters

As the proposed inverters are constructed of the series connection of an arbitrary number of basic units with a different number of DC voltage sources in each one, a different number of output voltage levels can be achieved. In this section, an

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optimal design of the proposed multilevel inverters is studied in various aspects, like maximizing the number of output voltage levels, while minimizing the number of switches, DC voltage sources, gate driver circuits, as well as minimizing *TSV*. Optimal structures are presented separately for each proposed multilevel inverter discussed in the previous section.

A. Optimal Structures of the First Proposed Multilevel Inverter

In this subsection, four optimization scenarios are presented to optimize the first proposed inverter.

1) Achieving the maximum number of the output voltage levels in terms of a constant number of switches

The total number of IGBTs used in the proposed multilevel inverter is the summation of the number of IGBTs in each basic unit. One can write,

$$N_{IGBT} = 4 \times \left(\sum_{i=1}^{k} n_i \right), \tag{22}$$

where n_i is a natural number and $N_{IGBT} = cte$. According to (16), the maximum number of the output voltage levels is the multiplication of some natural numbers, so this multiplication will be maximized if each number of it is maximized. In this case, the maximum value of each number is limited by (22); therefore, the following equation must be valid,

$$n_1 = n_2 = \cdots = n_k = n. \tag{23}$$

According to (23) and (16), one can write,

$$N_{step} = [n(n+1)+1]^k. \tag{24}$$

As $n = \frac{N_{IGBT}}{4k}$, according to (24) we have,

$$N_{step} = \left\{ [n(n+1)+1]^{\frac{1}{4n}} \right\}^{N_{IGBT}}. \tag{25}$$

The maximum value of (25) occurs if expression $[n(n+1)+1]^{\frac{1}{4n}}$ maximizes. This expression is illustrated in Fig. 4(a) in terms of *n*. It can be observed that the maximum number of output voltage levels can be obtained when *n*=2.

2) Achieving the maximum number of the output voltage levels in terms of a constant number of gate driver circuits

One of the design goals in multilevel inverters is to obtain the maximum value of N_{step} by maintaining the number of gate driver circuits (N_{driver}) constant. The number of gate driver circuits for the proposed multilevel inverter is as follows,

$$N_{driver} = 3 \times \left(\sum_{i=1}^{k} n_i \right) + k. \tag{26}$$

According to (16) and (26), N_{step} will be maximized if the number of DC voltage sources of the basic units is the same to each other. In this way, one can write,

$$k = \frac{N_{driver}}{3n+1}. \tag{27}$$

According to (24) and (27), we have,

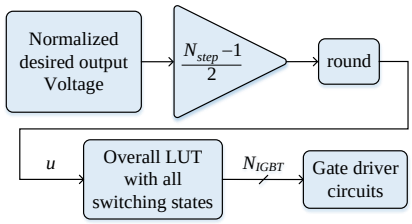

Fig. 3. The utilized modulation scheme diagram.

TABLE II
AN EXAMPLE OF THE OVERALL LUT USED TO MODULATE THE PROPOSED INVERTER IN THE POSITIVE HALF-CYCLE OF THE OUTPUT VOLTAGE PERIOD.

Output voltage level	1st B.U. Sw. states	2nd B.U. Sw. states	V_{O1}	V_{O2}	V_O
24	3	3	3×*V*	21×*V*	24×*V*
23	2		2×*V*		23×*V*
22	1		*V*		22×*V*
21	0		0		21×*V*
20	-1		- *V*		20×*V*
19	-2		-2×*V*		19×*V*
18	-3		-3×*V*		18×*V*
17	3	2	3×*V*	14×*V*	17×*V*
16	2		2×*V*		16×*V*
15	1		*V*		15×*V*
14	0		0		14×*V*
13	-1		- *V*		13×*V*
12	-2		-2×*V*		12×*V*
11	-3		-3×*V*		11×*V*
10	3	1	3×*V*	7×*V*	10×*V*
9	2		2×*V*		9×*V*
8	1		*V*		8×*V*
7	0		0		7×*V*
6	-1		- *V*		6×*V*
5	-2		-2×*V*		5×*V*
4	-3		-3×*V*		4×*V*
3	3	0	3×*V*	0	3×*V*
2	2		2×*V*		2×*V*
1	1		*V*		*V*
0	0		0		0

B.U.=Basic Unit, Sw.=Switch.

$$N_{step} = \left\{ [n(n+1)+1]^{\frac{1}{3n+1}} \right\}^{N_{driver}}. \tag{28}$$

If expression $[n(n+1)+1]^{\frac{1}{3n+1}}$ has the maximum value, N_{step} will be maximized. In Fig. 4(b), this expression is depicted. It can be observed that the maximum value of this expression will be achieved by selecting *n*=2.

3) Achieving the maximum number of the output voltage levels in terms of a constant number of DC voltage sources

Another design aim is to maximize N_{step} while maintaining the total number of DC voltage sources (N_{DC}) constant for the proposed multilevel inverter,

$$N_{DC} = \sum_{i=1}^{k} n_i = cte. \tag{29}$$

According to (16) and (29), the N_{step} will gain its maximum value, if the number of DC voltage sources in basic units is identical to each other. As a result, we will have,

$$k = \frac{N_{DC}}{n}. \tag{30}$$

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Substituting (30) into (24) gives,

$$N_{step} = \left\{[n(n+1)+1]^{\frac{1}{n}}\right\}^{N_{DC}}. \quad (31)$$

In this case, the maximum number of output voltage levels can be achieved by selecting n=2.

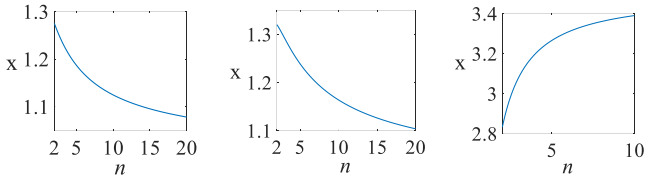

Fig. 4. Variation of some functions in terms of n. (a) Variation of $[n(n+1)+1]^{\frac{1}{4n}}$, (b) $[n(n+1)+1]^{\frac{1}{3n+1}}$, and (c) $\frac{7n^2+5n-4}{2n(n+1)}$.

4) Achieving minimum TSV in terms of a constant number of the output voltage levels

In this scenario, the objective is to minimize the *TSV* while maintaining the number of output voltage levels constant. In this regard, the structure that provides the lowest *TSV* would be optimum.

In this case, (4) need to be modified as,

$$V_{S_{j,1}-S_{j,4}} = \sum_{i=1}^{n_j} V_{j,i} \ , \begin{cases} V_{S_{l,j,i}} = V_{j,(i+1)} \\ V_{S_{m,j,i}} = V_{j,(i+1)}, \\ V_{S_{u,j,i}} = V_{j,i} \end{cases} \quad (32)$$
$$j = 1,2,\dots,k, \qquad i = 1,2,\dots,n_j - 1.$$

The *TSV* is given by

$$TSV = \sum_{j=1}^{k}\left\{\left[\frac{7n_j^2+5n_j-4}{2}\right]\times\prod_{i=1}^{j-1}\left[n_j(n_j+1)+1\right]\right\}V. \quad (33)$$

Substituting (23) into (33) gives

$$TSV = \frac{7n^2+5n-4}{2n(n+1)}\times\left[N_{step}-1\right]\times V. \quad (34)$$

As shown in Fig. 4(c), it can be observed that by selection of n=2 the *TSV* will be minimized.

B. Optimal Structures of the Second Proposed Multilevel Inverter

The scenarios presented in the previous subsection are repeated for the second proposed inverter as follows,

1) Achieving the maximum number of the output voltage levels in terms of a constant number of switches

In this case (22) is assumed to be constant and (21) need to be maximized, so it can be concluded that (23) should be satisfied. As a result, one can write,

$$N_{step} = (2^{n+1}-1)^k. \quad (35)$$

Substituting $k = \frac{N_{IGBT}}{4n}$ in (35) gives,

$$N_{step} = \left[(2^{n+1}-1)^{\frac{1}{4n}}\right]^{N_{IGBT}}. \quad (36)$$

According to (36), N_{step} is maximized if expression $(2^{n+1}-1)^{\frac{1}{4n}}$ is maximized. Fig. 5(a) shows this expression in terms of n. By using two DC voltage sources in each basic unit the N_{step} will be maximized.

2) Achieving the maximum number of the output voltage levels in terms of a constant number of gate driver circuits

According to (21) and (26), it can be concluded that by assuming a constant N_{driver}, if (23) satisfies, N_{step} will be maximized. Substituting $k = \frac{N_{driver}}{3n+1}$ into (21) yields

$$N_{step} = \left[(2^{n+1}-1)^{\frac{1}{3n+1}}\right]^{N_{driver}}. \quad (37)$$

So, by using two DC voltage sources in each basic unit, N_{step} will be maximized while the N_{driver} is constant.

3) Achieving the maximum number of the output voltage levels in terms of a constant number of DC voltage sources

According to (21) and (29), the N_{step} of the proposed inverter can be found when the number of DC voltage sources in each basic unit is identical. Substituting (30) into (35) gives,

$$N_{step} = (2^{n+1}-1)^{\frac{N_{DC}}{n}}. \quad (38)$$

So, using two DC voltage sources (n=2) in each basic unit results in maximum N_{step}.

4) Achieving minimum TSV in terms of a constant number of output voltage levels

In this scenario, according to (35) the *TSV* is as follows,

$$TSV = \left[2+\frac{5(2^n-2)}{4(2^n-1)}\right]\times\left[N_{step}-1\right]\times V. \quad (39)$$

The minimum value of the *TSV* can be obtained by minimizing expression $\left(2+\frac{5(2^n-2)}{4(2^n-1)}\right)$. Fig. 5(b) shows this expression as a function of n. As it can be observed, again by using two DC voltage sources (n=2) in each basic unit, the minimum value of the *TSV* will be obtained.

From previous sections, one can find that the proposed inverter will be optimum in all aspects if the number of DC voltage sources in each basic unit equals to two. This fact is an advantage for the proposed multilevel inverters.

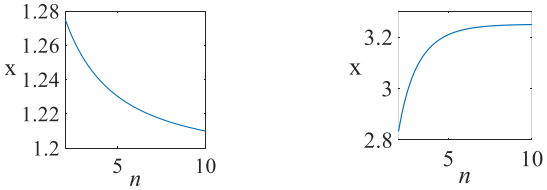

Fig. 5. Variation of some functions in terms of n. (a) Variation of $(2^{n+1}-1)^{\frac{1}{4n}}$, (b) $\left(2+\frac{5(2^n-2)}{4(2^n-1)}\right)$.

V. Comparison With Other Topologies

In this section, the proposed inverters are compared with recently presented topologies in the literature. Optimal structure of the proposed multilevel inverters is considered to have a fair comparison with other inverters. In other words, the number of DC voltage sources in each basic unit is two (n=2).

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TABLE III
IGBTS WITH DIFFERENT VOLTAGE RATINGS

IGBT module	CM400D U-5F	IKW75N 60T	IGW60T1 20	FZ600R1 7KE4
Rating [V]	250	600	1200	1700
IGBT module	IXCH 36N250	FZ400R33 KL2C_B5	FZ800R45 KL3_B5	FZ250R6 5KE3
Rating [V]	2500	3300	4500	6500

The first and second proposed multilevel inverters are known as P_1 and P_2, respectively. For comparison purpose, the symmetric and asymmetric CMI are named as R_1 and R_2, and the multilevel inverters presented in [13]-[17] are indicated by R_3-R_7, respectively.

In Fig. 6(a), N_{DC} is shown in terms of N_{step}, where the proposed multilevel inverters have the lowest number of the DC voltage sources than other topologies. Number of IGBTs versus N_{step} is shown in Fig. 6(b). As shown, the proposed multilevel inverters have the lowest N_{IGBT} among other topologies for N_{step}>14. The multilevel inverter presented in [13] (R_3) has the lowest N_{driver} followed by proposed multilevel inverters, as shown in Fig. 6(c).

Fig. 6(d) shows that for the TSV index, the proposed multilevel inverters are placed in a moderate range. The rationale behind this fact is that the proposed multilevel inverters use H-bridge in each basic unit which causes a higher standing voltage on H-bridge IGBTs.

The ratio of the number of the output voltage levels to the IGBTs in terms of the number of DC voltage sources is shown in Fig. 6(e), where the inverters that can increase the number of DC voltage sources in each basic unit are considered.

As one can see, the proposed multilevel inverters have the highest ratio among other topologies. The rate of rising of the second proposed inverter is higher than the first one.

VI. MEDIUM-VOLTAGE APPLICATION CONCERNS

The proposed multilevel inverter uses an H-bridge in the load side of each basic unit. The H-bridge rated voltage is equal to the sum of DC voltage sources of the corresponding basic unit. This rated voltage increases, as the number of output voltage levels does. Considering commercially available IGBTs shown in Table III, high voltage applications lead to series connection of IGBTs in H-bridges. This causes the proposed multilevel inverter does not present its advantages in high-voltage applications. It is worth mentioning, the presented inverters in [13] and [15]-[17] have the same limitation.

To avoid series connection of switches, it is essential to determine which H-bridge has the highest standing voltage. According to (15) and (20), one can find that the H-bridge of the k^{th} basic unit (the last basic unit) has the highest standing voltage. Therefore, if (40) satisfies, there is no need to series connection of IGBTs in the proposed inverter.

$$v_{H,rated}^{k} = \frac{v_{IGBT,rated}}{\beta}, \tag{40}$$

where, $v_{H,rated}^{k}$, $v_{IGBT,rated}$, and β are the rated voltage of the k^{th} H-bridge, the highest rated voltage IGBT used in the inverter, and switch's voltage safety factor, respectively. The rated voltage of the application in which the utilization of the proposed inverter justifies can be obtained as follows,

$$V_{LL,rated} = \sqrt{\frac{3}{2}} \times \sum_{j=1}^{k} v_{H,rated}^{j}, \tag{41}$$

where, $V_{LL,rated}$ is the rated line-line RMS voltage of load/grid in a three-phase system. For optimal structure ($n_1 = n_2 = \cdots = n_k = n$), and from (15) and (20) one can find,

$$V_{LL,rated} = \sqrt{\frac{3}{2}} \times \frac{(n(n+1)+1)^k - 1}{2} \times V. \tag{42}$$

$$V_{LL,rated} = \sqrt{\frac{3}{2}} \times \frac{(2^{n+1}-1)^k - 1}{2} \times V. \tag{43}$$

Equations (42) and (43) are obtained based on the first and second proposed multilevel inverters equations (in section III), respectively.

First example- It is assumed that the highest available rated voltage of IGBT is 4.5kV (Table III). Considering the optimal structure (n_j=2) with two series connected basic units to form a 49-level output voltage and β=1.7. Using (40), the second H-bridge rated voltage will be 2.6kV. The smallest DC source voltage is $V_{1,1}$= 126V and the $V_{LL,rated}$ =3.7kV. Other DC voltage sources are $V_{1,2}$=252V, $V_{2,1}$=882V, and $V_{2,2}$=1764V. According to Table III, one 600V IGBT for $S_{u1,1}$, three 1200V IGBTs for $S_{m1,1}$, $S_{l1,1}$, and $S_{u2,1}$, four 1200V IGBTs for $S_{1,1}$-$S_{1,4}$, two 2500V IGBTs for $S_{m2,1}$ and $S_{l2,1}$, and four 4500V IGBTs for $S_{2,1}$-$S_{2,4}$ are required.

Second example- It is assumed that the proposed inverter is connected to a three-phase 7kV system. The amplitudes of DC voltage sources will be: $V_{1,1}$=238.1V, $V_{1,2}$=476.2V, $V_{2,1}$=1667 V, and $V_{2,2}$=3333V. The rated voltage of the second H-bridge is 5kV and the highest rated voltage of IGBT is 8.5kV. According to Table III, three 600V IGBTs for $S_{u1,1}$, $S_{m1,1}$, and $S_{l1,1}$, four 1200V IGBTs for $S_{1,1}$-$S_{1,4}$, one 2500V IGBT for $S_{u2,1}$, and two 4500V IGBTs for $S_{m2,1}$ and $S_{l2,1}$ are required. In addition, each $S_{2,1}$-$S_{2,4}$ consists of two series connected 4500V IGBTs. As a result, with today's semiconductor technology the

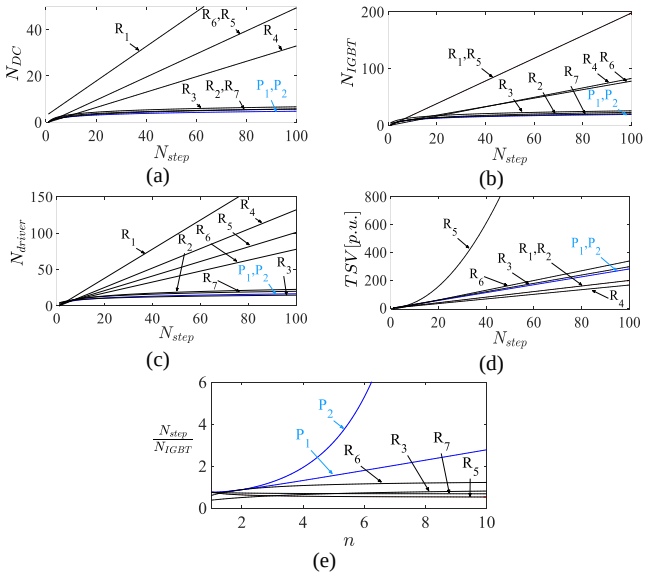

Fig. 6. Comparing the proposed inverters with recent topologies. (a) N_{DC}, (b) N_{IGBT}, (c) N_{driver}, (d) *TSV* in terms of N_{step}, and (e) $\frac{N_{step}}{N_{IGBT}}$ in terms of n.

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proposed multilevel inverter and those presented in [13], [15]-[17] have limitation in high-voltages and they are suited for low- to medium-voltage applications.

VII. Simulation And Experimental Results

A. Simulation Results

To examine the performance of the proposed inverters through simulation, a 49-levels structure consists of two basic units with two DC voltage sources in each one (optimal structure) is considered. System specifications for simulation are shown in Table IV. The maximum standing voltage of switches belongs to the H-bridge of second basic unit; according to Table IV and (4), this value is 1050V. Considering the switch voltage safety factor (β) of 1.7, so the maximum standing voltage of the inverter is about 1800V. For simplicity purpose, all switches used in simulations are identical and have the rated voltage of 1800V.

Output voltage waveforms of the first and second H-bridges along with the output voltage and current waveforms of the proposed inverter are illustrated in Fig. 7. As shown, the output voltage is the summation of the first and second basic units' voltages. According to Table II, DC voltage sources of the first basic unit have to subtract from the second basic unit DC voltage sources in some instances to maintain the uniformity of the output voltage waveform (V_O). This is due to the lower amplitude of the first basic unit DC voltage sources than the second one. Therefore, V_{O1} waveform has a different shape from V_{O2}. For the time interval of 0-40ms, the modulation index (m) is 1 and both basic units generate their maximum number of voltage levels which is 49. In the next time interval (40-80ms), the modulation index changes from 1 to 0.2 and it can be seen that the inverter decreases its number of voltage levels in both basic units to reach the requested voltage at its output terminal (11-levels). At the final time interval of 80-120ms, the modulation index increases from 0.2 to 0.6 and the number of output voltage levels changes to 29. Accordingly, the ability of the proposed modulation scheme to generate output voltage with a desire number of levels and amplitude at different modulation indices is verified. Achieving output voltage (current) with a THD of 1.65% (0.09%) for 49-levels output voltage confirms that the proposed inverter can produce high-quality sinusoidal output voltages.

Modular multilevel converter (MMC) is one of the multilevel inverter topologies that has attracted much attention among the researchers and industry in the last decade and is commercial [19]. The MMC is thoroughly investigated in [20]. A comparison between the proposed inverter and the MMC in term of various aspects for a single-phase system is illustrated in Table V. It is important to note that the number of switches in Table V for each inverter is the minimum number that the inverter requires to operate properly and the voltage rating of the switches are considered in the *TSV* of each inverter. To have a better comparison, two cases are considered.

In the first case, the number of switches used in both inverters is 16. In the second case, the number of output voltage levels of both inverters is 7. Specifications of the proposed inverter in the first case are same as the Table IV (two basic units with two DC sources in each one). Therefore, the maximum output voltage amplitude of the proposed inverter is 1200V. To perform a fair comparison with the same conditions, the MMC's DC link voltage have to be 2400V and its output active power is set to 100kW. The MMCs use eight and twelve half-bridge cells in the first and second cases, respectively. The proposed inverter contains two (one) basic units (unit) with four (two) DC voltage sources to generate a 49-level (7-level) output voltage in the first (second) case. According to Table V, following statements can be concluded: the MMC has a single DC source while, the proposed inverter requires multiple asymmetric DC sources. The MMC has many floating capacitors to generate multilevel output voltage, but the proposed inverter has no floating capacitor. In the first case, the proposed inverter has a much higher number of output voltage levels than the MMC; if it is desire to generate a 49-level output voltage, the MMC must have 96 half-bridge cells (192 switches), while the proposed inverter utilizes 16 switches. In the second case, the proposed inverter has much lower number of switches than the MMC; if it is desire to use 8 switches, the MMC will generate a 3-level output voltage, while the proposed inverter has a 7-level output voltage. The proposed inverter has lower *TSV* than the MMC (≈29% reduction). On the other hand, the proposed inverter and those presented in [13] and [15]-[17] do not have the same modular design as the MMC do.

To simulate the MMC, the capacitance of the floating capacitors of each cell is 2mF and the inductance of the arm inductors is 8mH. In Fig. 8, losses and efficiency of the proposed inverter are compared with the MMC in terms of the active output power, power factor, and modulation index variations. Losses evaluation process used in the simulation can be found in [21] and the parameters required to calculate the

TABLE IV
PROPOSED INVERTER SPECIFICATIONS FOR SIMULATION

Output active power (kW)	100
Output reactive power (kVar)	50
Number of basic units	2
DC voltage sources	$V_{1,1}$=50V, $V_{1,2}$=100V $V_{2,1}$=350V, $V_{2,2}$=700V
Rated voltage of utilized IGBTs ($V_{CE,rated}$)	1800V
Modulation index	1

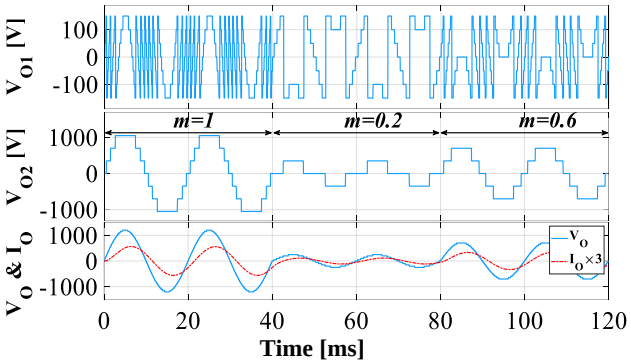

Fig. 7. Output voltages and current of the simulated proposed inverter, the output voltage of the first basic unit (upper), second basic unit (middle), and inverter output voltage and current (lower).

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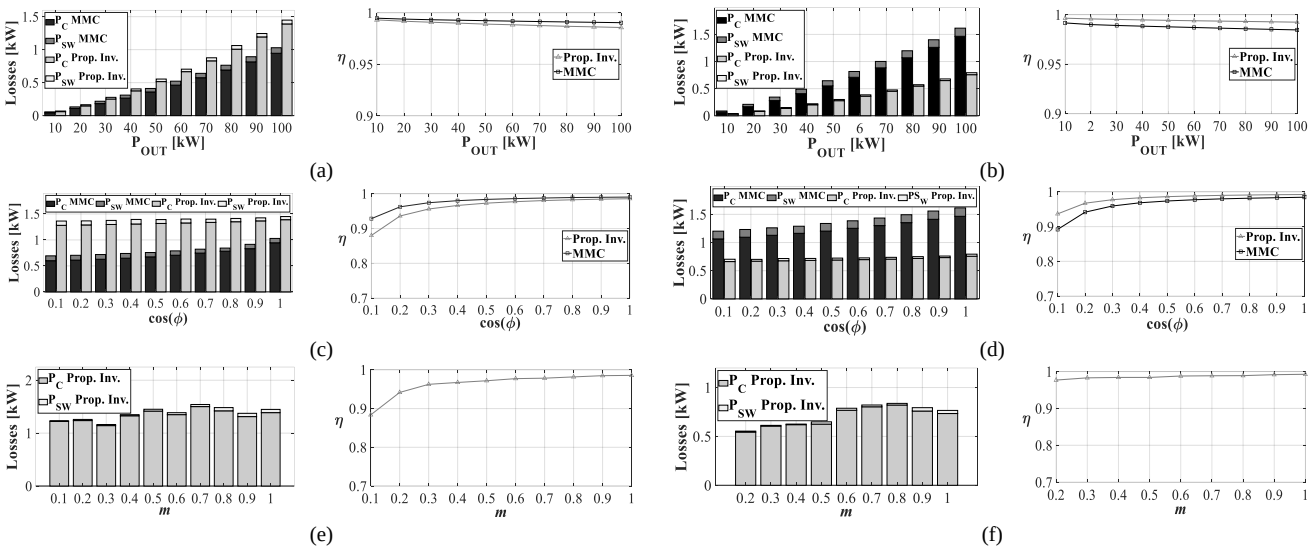

Fig. 8. Losses and efficiency evaluation of the proposed inverter and the MMC in term of (a) the output power for the first case, (b) the output power for the second case, (c) the power factor for the first case, (d) the power factor for the second case, (e) the modulation index for the first case, and (f) the modulation index for the second case.

losses are taken from [22]. IGBTs with the same specifications are used to simulate both converters. The proposed inverter and the MMC are simulated by a same NLC modulation method. Fig. 8 (a, c, and e) show results for the first case and Fig. 8 (b, d, and f) show the second case results. In Fig. 8 (a)-(b), the output active power is increased from 0.1 p.u. to 1.0 p.u., the modulation index is set to one, and the reactive output power is set to zero. It can be observed that the losses of the proposed inverter is higher than the MMC in the first case, while in the second case the proposed inverter has lower losses than the MMC. In addition, the efficiency of the proposed inverter in the second case is higher than the efficiency of the MMC in the first case. In Fig. 8 (c)-(d), the power factor varies from 0.1 lagging to 1, where the apparent output power of the inverter is kept constant (S=100kVA) and the modulation index is set to one. It can be observed that an increase of the output power factor causes an increase in both losses and efficiency. This is due to decrease of the output current amplitude by increase of the output power factor.

In Fig. 8 (e)-(f), the modulation index varies from 0.1 to 1. In this case, the amplitude of output current is kept constant (according to output active power of 100kW) and the output power factor is set to be one. Only results of the proposed inverter are shown in this figure, since the capacitor voltage ripple of the MMC become very large in low modulation indices such that the MMC loses its normal operation. It is observed that, losses do not uniformly increase by modulation index. The rationale behind this is that the number of on-state switches non-uniformly varies by variation of the modulation index in each instant. It worth mentioning that in Fig. 8 (f) the modulation index starts from 0.2, because the modulator creates zero signal when the modulation index is lower than 0.167 for a 7-level inverter.

TABLE V
COMPARISON BETWEEN THE PROPOSED MULTILEVEL INVERTER AND THE MMC

Inverter topology	Proposed inverter		MMC	
	1st case	2nd case	1st case	2nd case
Num. of switches	**16**	8	**16**	24
Num. of output voltage levels	49	**7**	5	**7**
Num. of DC voltage sources	4	2	1	1
Num. of floating capacitors	0	0	8	12
TSV	6800V		9600V	

B. Experimental Results

An experimental setup is prepared to validate the proposed inverter operation. This setup is shown in Fig. 9 (a) and consists of one basic unit with two DC voltage sources. Specifications of the setup are shown in Table VI. Harmonic specifications of the output voltage captured from a power analyser instrument are shown in Fig. 9 (b). In this figure, U_{thd}, U_{hc}, and U_{fc} are calculated as,

$$U_{thd}=\frac{\sqrt{U_{RMS}^2-U_{H01}^2}}{U_{H01}}, U_{hc}=\frac{\sqrt{U_{RMS}^2-U_{H01}^2}}{U_{RMS}}, U_{fc}=\frac{U_{H01}}{U_{RMS}}, \quad (44)$$

where, U_{H01} and U_{RMS} are the amplitude of the fundamental frequency component and the RMS value of the output voltage, respectively. U_{hc} and U_{fc} show harmonic and fundamental content of the output voltage, respectively. As shown in figure, power quality indices of the output voltage confirm good quality of the proposed inverter.

Output voltage and current waveforms are depicted in Fig. 10. As it can be observed the output voltage has 7-levels. Voltage and current waveforms of switches $S_{u1,1}$, $S_{m1,1}$, $S_{l1,1}$ and $S_{1,1}$ are shown in Fig. 11(a-d), respectively. As shown, switches voltage is deferent from the voltage of DC voltage sources in the zero output voltage level. The rationale behind this is the presence of off-state resistance of switches in zero output voltage level. The equivalent circuit of the proposed inverter in the zero output voltage level is shown in Fig. 12, where all switches are considered to be the same. In this figure, R_{off} is the off-state resistance of switches. Solving the circuit shown in

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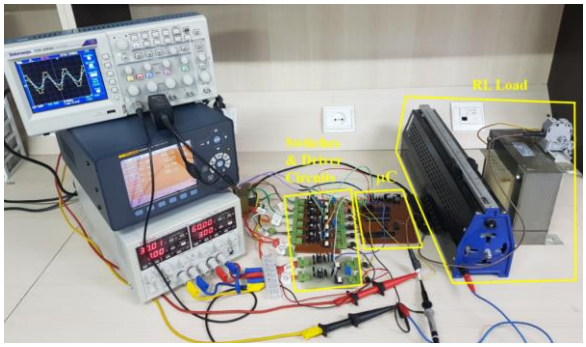

(a)

(b)

Fig. 9. An overview of the experimental setup. (a) Overall setup, and (b) Harmonic specifications of the proposed inverter output voltage.

TABLE VI
EXPERIMENTAL SETUP SPECIFICATIONS

Output active Power (W)	440
Output reactive Power (Var)	80
DC sources voltage (V)	30, 60
MOSFETs Spec.	IRF740, 400V, 10A
Modulation Index	1

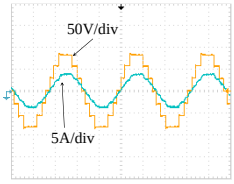

Fig. 10. Output voltage and current waveforms.

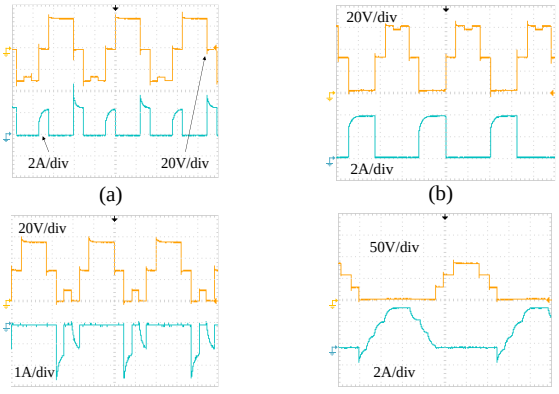

Fig. 11. Switch's voltage and current waveforms of (a) $S_{u1,1}$, (b) $S_{m1,1}$, (c) $S_{l1,1}$, and (d) $S_{1,1}$.

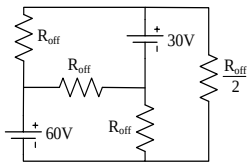

Fig. 12. The equivalent circuit of the proposed inverter in zero output voltage level.

Fig. 12, yields the voltage of switches as demonstrated in Table VII. As one can see, analytical voltages in zero output voltage level are consistent with those shown in Fig. 11.

TABLE VII
THE VOLTAGE OF SWITCHES IN THE ZERO OUTPUT VOLTAGE LEVEL

$V_{Su1,1}$ (V)	$V_{Sm1,1}$ (V)	$V_{Sl1,1}$ (V)	$V_{S1,2}$ (V)	$V_{S1,1}$ (V)
-24	54	6	36	0

VIII. CONCLUSION

An asymmetric multilevel inverter composed of cascaded connection of the basic units is proposed with a reduced number of components. According to the simulation and experimental results, and comparison with recently presented multilevel inverter topologies, in the proposed inverter the number of components is considerably reduced. It is shown that the proposed inverter has a lower number of DC voltage sources, IGBT switches, and gate driver circuits and the highest ratio of output voltage level number to IGBT number (N_{step}/N_{IGBT}) than some recently presented multilevel inverters in literature. The proposed inverter has a lower total standing voltage and switching loss than the modular multilevel converter (MMC). The optimal topology of the proposed inverter in various design goals is achieved by using two DC voltage sources in each basic unit, which is an outstanding advantage. The proposed inverter is well suited for low- to medium-voltage applications, where it shows the advantage of a higher power quality and a lower number of components.

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